

TYPES SN54178, SN54179, SN74178, SN74179 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

DECEMBER 1972—REVISED DECEMBER 1983

- Typical Maximum Clock Frequency . . . 39 MHz
- Three Operating Modes:
Synchronous Parallel Load
Right Shift
Hold (Do Nothing)
- Negative-Edge-Triggered Clocking
- D-C Coupling Simplifies System Designs

description

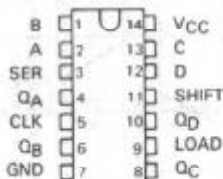
These shift registers utilize fully d-c coupled storage elements and feature synchronous parallel inputs and parallel outputs. The SN54179/SN74179 has a direct clear line and complementary output from the D flip-flop, thereby differing from the SN54178/SN74178.

Parallel loading is accomplished by taking the shift input low, applying the four bits of data, and taking the load input high. The data is loaded into the associated flip-flop synchronously and appears at the outputs after a high-to-low transition of the clock. During loading, serial data flow is inhibited.

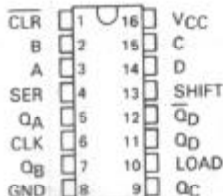
Shift right is also accomplished on the falling edge of the clock pulse when the shift input is high regardless of the level of the load input. Serial data for this mode is entered at the serial data input.

When both the shift and load inputs are low, clocking of the register can continue; however, data appearing at each output is fed back to the flip-flop input creating a mode in which the data is held unchanged. Thus, the system clock may be left free-running without changing the contents of the register.

SN54178 . . . J OR W PACKAGE
SN74178 . . . J OR N PACKAGE
(TOP VIEW)



SN54179 . . . J OR W PACKAGE
SN74179 . . . J OR N PACKAGE
(TOP VIEW)



'178, '179†
FUNCTION TABLE

INPUTS					OUTPUTS				
CLEAR†	SHIFT	LOAD	CLOCK	SERIAL	PARALLEL				Q _D †
					A	B	C	D	
L	X	X	X	X	X	X	X	X	H
H	X	X	H	X	X	X	X	X	Q _{A0} Q _{B0} Q _{C0} Q _{D0}
H	L	L	↓	X	a	b	c	d	Q _{A0} Q _{B0} Q _{C0} Q _{D0}
H	L	H	↓	X	a	b	c	d	Q _{A0} Q _{B0} Q _{C0} Q _{D0}
H	H	X	↓	H	X	X	X	X	Q _{A0} Q _{B0} Q _{C0} Q _{D0}
H	H	X	↓	L	X	X	X	X	Q _{A0} Q _{B0} Q _{C0} Q _{D0}

† The columns for clear, Q_D, and the top line of the table apply for the '179 only.

H = high level (steady state), L = low level (steady state)

X = irrelevant (any input, including transitions)

↓ = transition from high to low level

a, b, c, d = the level of steady state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most-recent ↓ transition of the clock.

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

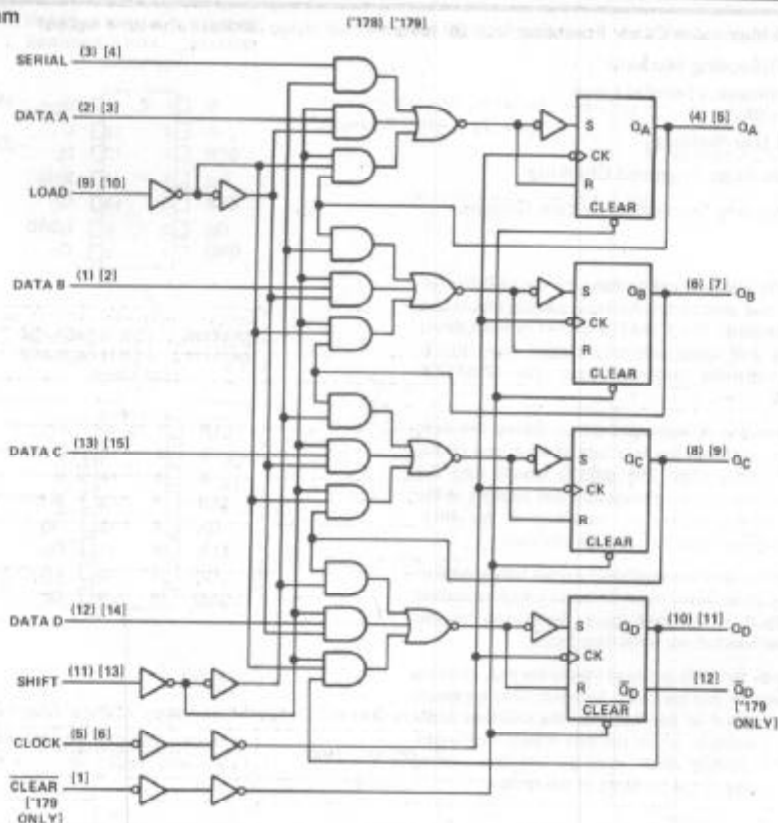
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

3

TTL DEVICES

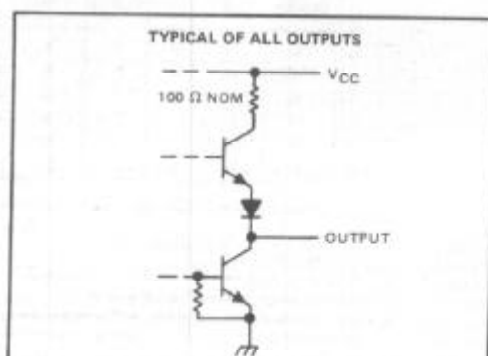
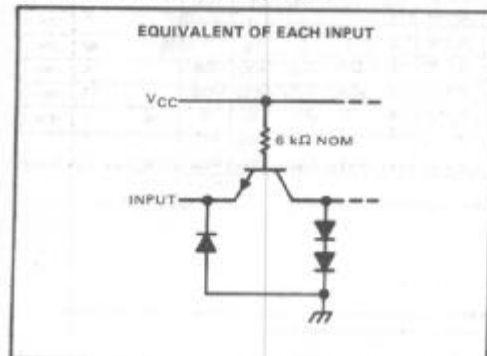
TYPES SN54178, SN54179, SN74178, SN74179 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

logic diagram



Pin numbers shown on logic notation are for J or N packages.

schematics of inputs and outputs



TYPES SN54178, SN54179, SN74178, SN74179 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature: SN54178, SN54179 Circuits	-55°C to 125°C
SN74178, SN74179 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54178, SN54179			SN74178, SN74179			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}					-800			-800	μ A
Low-level output current, I_{OL}					16			16	mA
Clock frequency, f_{clock}			0		25	0		25	MHz
Width of clock or clear pulse, t_W (see Figure 1)					20			20	ns
Setup time, t_{SU} (see Figure 1)		Shift (H or L) or load			35			35	ns
		Data			30			30	
		Clear-inactive-state (SN54179 and SN74179)			15			15	
Hold time at any input, t_H					5			5	ns
Operating free-air temperature, T_A					-55			125	0 70 °C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54178, SN54179			SN74178, SN74179			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-20		-57	-18		-57	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2	46	70		46	75		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured as follows:

- 4.5 V is applied to serial inputs, load, shift, and clear.
- Parallel inputs A through D are grounded.
- 4.5 V is momentarily applied to clock which is then grounded.

TYPES SN54178, SN54179, SN74178, SN74179 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

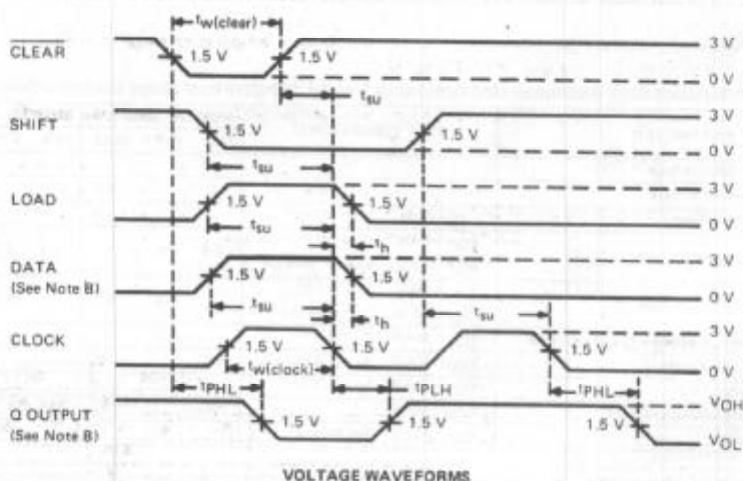
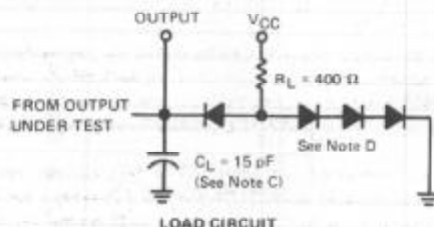
PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			$C_L = 15\text{ pF}, \quad R_L = 400\ \Omega,$ See Figure 1	25	39		MHz
t_{PLH}	$\overline{\text{Clear}}$	$\overline{Q_D}$			15	23	ns
t_{PHL}		Q_A, Q_B, Q_C, Q_D			24	36	
t_{PLH}	Clock	Any output			17	26	ns
t_{PHL}						23	

[†] f_{max} = Maximum clock frequency

t_{PHL} = Propagation delay time, high-to-low-level output

t_{PLH} = Propagation delay time, low-to-high-level output

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Input pulses are supplied by generators having the following characteristics: $t_{PLH} < 10\text{ ns}$, $t_{PHL} < 10\text{ ns}$, $PRR < 1\text{ MHz}$, $Z_{out} \approx 50\ \Omega$.
- B. Data input and Q output are any related pair. Serial and other data inputs are at GND. Serial data input is tested in conjunction with Q_A output in the shift mode.
- C. C_L includes probe and jig capacitance.
- D. All diodes are 1N3064 or equivalent.

FIGURE 1—SWITCHING TIMES

TYPES SN54180, SN74180 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

DECEMBER 1972—REVISED DECEMBER 1983

FUNCTION TABLE

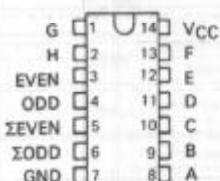
INPUTS			OUTPUTS	
Σ OF H's AT A THRU H	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	H	L	H	L
ODD	H	L	L	H
EVEN	L	H	L	H
ODD	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = high level, L = low level, X = irrelevant

SN54180 ... J OR W PACKAGE

SN74180 ... J OR N PACKAGE

(TOP VIEW)



description

These universal, monolithic, 9-bit (8 data bits plus 1 parity bit) parity generators/checkers, utilize familiar Series 54/74 TTL circuitry and feature odd/even outputs and control inputs to facilitate operation in either odd or even-parity applications. Depending on whether even or odd parity is being generated or checked, the even or odd inputs can be utilized as the parity or 9th-bit input. The word-length capability is easily expanded by cascading.

The SN54180/SN74180 are fully compatible with other TTL or DTL circuits. Input buffers are provided so that each data input represents only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs at a low logic level. A fan-out to 20 normalized loads is provided at a high logic level to facilitate the connection of unused inputs to used inputs. Typical power dissipation is 170 mW.

The SN54180 is characterized for operation over the full military temperature range of -55°C to 125°C ; and the SN74180 is characterized for operation from 0°C to 70°C .

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54180 Circuits	-55°C to 125°C
SN74180 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54180			SN74180			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}\text{C}$

TEXAS
INSTRUMENTS

POST OFFICE BOX 225012 • DALLAS, TEXAS 75285

3-705

3

TTL DEVICES

TYPES SN54180, SN74180 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54180			SN74180			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -800 \mu\text{A}$	2.4	3.3		2.4	3.3		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$		1			1		mA
I_{IH} High-level input current	Any data input		40			40		μA
	Even or odd input		80			80		
I_{IL} Low-level input current	Any data input		-1.6			-1.6		mA
	Even or odd input		-3.2			-3.2		
I_{OS} Short-circuit output current‡	$V_{CC} = \text{MAX}$	-20	-55	-18	-55	-55	-18	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2	34	49		34	56		mA

NOTE 2: I_{CC} is measured with even and odd inputs at 4.5 V, all other inputs and outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

§Not more than one output should be shorted at a time.

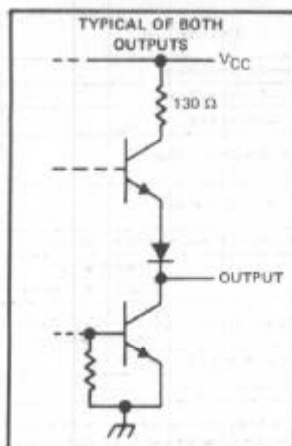
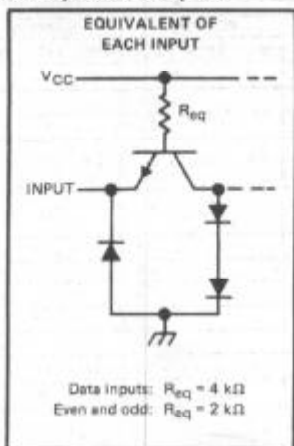
switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Σ Even	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, Odd input grounded, See Note 3	40	60		ns
t_{PHL}		Σ Odd		45	68		
t_{PLH}	Data	Σ Even	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, Even input grounded, See Note 3	32	48		ns
t_{PHL}		Σ Odd		25	38		
t_{PLH}	Data	Σ Even	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, Even input grounded, See Note 3	32	48		ns
t_{PHL}		Σ Odd		25	38		
t_{PLH}	Even or Odd	Σ Even or Σ Odd	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, See Note 3	40	60		ns
t_{PHL}		Σ Even or Σ Odd		45	68		
				7	10		ns

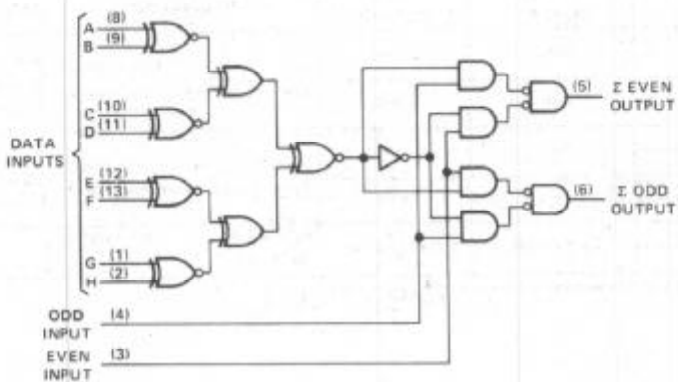
NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54180, SN74180 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

schematics of inputs and outputs



logic diagram *



Pin numbers shown on logic notation are for J or N packages.

3

TTL DEVICES